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BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,193	BAIN, PETER	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on August 22, 2003.

2. Claims 1-39 are examined.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on March 24, 2006 is being considered.

Oath/Declaration

4. The Office acknowledges receipt of properly signed oath/declaration filed August 22, 2003.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Regarding claims 1, 13, and 25, the phrase "substantially" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

7. Claims 1, 13, and 25 recite the limitation "the accuracy". There is insufficient antecedent basis for this limitation in the claims.

8. Claims 1, 13, and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear the word “accuracy” represent in the simulation result.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 13, 25, and 39 are provisionally rejected on the ground of non-statutory double patenting over claims 1, 13, 24, and 34 of US Patent No. 7,107,567. Although the conflicting claims are not identical, they are not patentably distinct from each other because after analyzing the language of the claims, it is clear that claim 1 of the '567 patent is slightly broader than claim 1 of the instant application. With respect to adding obfuscation circuitry to produce an obfuscated version of the electronic design, the language and the disclosure of the instant application not only fail to distinguish it from the '567 patent, but indicate that it is merely a subset of the '567 patent.

Claims 1, 13, 24, and 34 of Patent No. 7,107, 567 contain every element of claim 1, 13, 25, and 39 of the instant application and thus anticipate the claims of the instant

application. Claims of the instant application therefore are not patently distinct from the earlier patent claims and as such are unpatentable over obvious-type double patenting. A later application claims is not patentably distinct from the earlier claim if the later claim is anticipated by the earlier claim.

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

11. Claims 1, 13, 25, and 39 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter, specifically there is no tangible result. The method and product claims only receive, and add but produce no tangible result.

12. Claim 39 recites "An IP core comprising: ...". It is not belong to one of the categories of invention that deemed to be the appropriate subject matter of a patent such as processes, machines, manufactures, and compositions of matter.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claim 39 is rejected under 35 U.S.C. 102(e) as being anticipated by Publication No. US 2002/0138244 A1 issued to Meyer et al.

As per Claim 39:

Meyer discloses an IP core comprising;

a programming version of the IP core for insertion in an electronic design developed using a specified EDA platform (analogous to "Accordingly, it is also the object of this invention to provide a system and method that simplifies soft IP model distribution by allowing one object file to be linked to any HDL simulator on a given platform architecture type (such as X86 or Sparc)." [0073]); and

a simulation model of the IP core for simulating operation of the IP core in the electronic design, wherein the simulation model comprises obfuscation circuitry absent in the programming version, which allows a hardware simulation result of the IP core but prevents direct compilation to produce practical hardware implementation of the IP core (analogous to "IP protection is generally superior to any simulator specific model compiler, because simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty."[0072]).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,080,257 issued to Jakubowski et al in view of Publication No. US 2002/0138244 A1 issued to Meyer et al.

As per Claim 1:

Jakubowski discloses a, the method comprising:

receiving a non-obfuscated version of the electronic design suitable for direct compilation to a practical hardware implementation of the electronic design (analogous to "The original digital good 122 represents the software product or data as originally produced, without any protection or code modifications." Col. 4 lines 5-7); and

adding obfuscation circuitry to produce an obfuscated version of the electronic design from which the simulation model can be created, wherein the obfuscation circuitry does not substantially impact the accuracy of the simulation results, but prevents practical implementation of the electronic design on a hardware device (analogous to "Generally speaking, the obfuscator 134 automatically parses the original digital good 122 and applies selected protection tools 136(1)-136(N) to various portions

of the parsed good in a random manner to produce the protected digital good 124." Col. 3 lines 64-67; Fig. 1 element 134).

Jakubowski fails to disclose method of producing a simulation model of an electronic design, which simulation model produces a hardware simulation result but cannot be directly compiled to produce a practical hardware implementation of the electronic design.

Meyer discloses producing a simulation model of an electronic design, which simulation model produces a hardware simulation result (analogous to "...electronic subsystem (soft IP model) coded in hardware description languages (HDL) is converted into one or more plurality of object libraries that are linked within an HDL simulator to execute system simulation." [0096]), but cannot be directly compiled to produce a practical hardware implementation of the electronic design (analogous to "IP protection is generally superior to any simulator specific model compiler, because simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty."[0072]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Jakubowski related to systems and methods for protecting digital goods, such as software with the teachings of Meyer related to a simulation method and apparatus, and, in particular, for converting and simulating electronic circuits coded in Hardware Description Languages (HDL). The motivation for doing so would have been more convenient to combine into one system

simulation a plurality of subsystems HDL models created by different enterprises [0058]. Hence a skilled artisan having access to the teaching of Jakubowski and Meyer would have knowingly modified the teaching of Jakubowski with Meyer.

As per Claim 2:

Meyer discloses a method as recited in claim 1, wherein the non-obfuscated version of the electronic design is provided in a HDL source format (analogous to "The final SoC system then comprises HDL description from many sources." [0006]).

As per Claim 3:

Meyer discloses a method as recited in claim 1, wherein the electronic design is a reusable IP core (analogous to "HDLs also allow definition of reused groups of statements as tasks or function." [0026]).

As per Claim 4:

Jakubowski discloses a method as recited in claim 1, wherein adding obfuscation circuitry comprises:

identifying a region for introduction of obfuscation circuitry in the non- obfuscated version of the electronic design (analogous to "At block 602, the tool identifies instructions in the software code that possibly modify registers or flags. These instructions are called "key instructions"." Col. 8 lines 45-53);

choosing a type of obfuscation circuitry for insertion (analogous to "...a tool selector 206 which selects various tools 136 to augment the selected segments for protection purpose." Col. 5 lines 61-64); and

inserting the chosen type of obfuscation circuitry into the identified region, thereby creating an obfuscated (analogous to "For each key instruction, the tool inserts an extra instruction that modifies a register R in deterministic fashion based on the key instruction." Col. 8 lines 54-56).

As per Claim 5:

Meyer discloses a method as recited in claim 4, wherein identifying a region for introduction of obfuscation circuitry comprises identifying in the non-obfuscated version of the electronic design logic of a type that is not removed by a synthesizer (analogous to "The conversion from specification to a logic gate level HDL model can be direct or, alternately, a procedural HDL model (sometimes called RTL or behavioral model) can first be created and the procedural HDL code can then be synthesized into a gate level HDL model." [0013]).

As per Claim 6:

Jakubowski fails expressly to disclose one or more flip-flops. However, this feature is, which is one or more flip-flops, deemed to be inherent to the Jakubowski system which stated as follows: "Separating detection and response makes it difficult for an attacker to discern what event or instruction set triggered the response." Col. 14 lines 36-38. Without having a flip-flop in the system of Jakubowski, it is impossible to triggered the response because a flip-flop is a trigger circuit.

As per Claim 7:

Meyer discloses a method as recited in claim 1, further comprising optimizing the obfuscated version of the electronic design to merge the obfuscation circuitry with

functional circuitry (analogous to "The preferred embodiment has the advantage that optimization and shrouding or obfuscation operations...." [0101]).

As per Claim 8:

Jakubowski discloses a method as recited in claim 1, wherein the obfuscation circuitry comprises circuitry that increases the size of the electronic design without changing its function and/or slows the speed of the electronic design without changing its function (analogous to "For instance, the producer/developer might request that any protection not increase the runtime of the product." Col. 6 lines 49-50).

As per Claim 9:

Jakubowski discloses a method as recited in claim 1, wherein adding obfuscation circuitry comprises:

at a first location, adding circuitry for scrambling an input signal by spreading out the input signal in time; and at a second location, adding circuitry for de-scrambling an output signal resulting from the circuitry for scrambling (analogous to "Boolean Check Obfuscation" col. 12 lines 40 -67 and continue to col. 13 lines 1-26).

As per Claim 10:

Jakubowski discloses a method as recited in claim 1, wherein adding obfuscation circuitry comprises: at a first location, adding circuitry for entangling multiple input signals to thereby spread out the input signals; and at a second location, adding circuitry for detangling an output signal resulting from the circuitry for entangling (analogous to "encryption/decryption" col. 12 lines 15-21).

As per Claim 11:

Jakubowski discloses a method as recited in claim 1, wherein the obfuscation circuitry comprises a XOR tree (col. 9 lines 16-23).

As per Claim 12:

Jakubowski discloses a method as recited in claim 1, wherein adding obfuscation circuitry is performed automatically (analogous to "Generally speaking, the obfuscator 134 automatically parses the original digital good 122 and applies selected protection tools 136(1)-136(N) to various portion of the parsed good in a random manner to produce the protected digital good 124." Col. 3 lines 64-67 and continues col. 4 line 1).

As per Claim 13:

Jakubowski discloses an apparatus comprising;

one or more processors (Fig. 1 element 132);

memory (Fig. 1 element 120); and

an obfuscation module for adding obfuscation circuitry (Fig. 1 element 134) to a non-obfuscated version of the electronic design to produce an obfuscated version of the electronic design from which the simulation model can be created, wherein the obfuscation circuitry does not substantially impact the accuracy of the simulation result, but prevents practical implementation of the electronic design on a hardware device (analogous to "Generally speaking, the obfuscator 134 automatically parses the original digital good 122 and applies selected protection tools 136(1)-136(N) to various portions of the parsed good in a random manner to produce the protected digital good 124." Col. 3 lines 64-67).

Jakubowski fails to disclose method of producing a simulation model of an electronic design, which simulation model produces a hardware simulation result but cannot be directly compiled to produce a practical hardware implementation of the electronic design.

Meyer discloses producing a simulation model of an electronic design, which simulation model produces a hardware simulation result (analogous to "...and electronic subsystem (soft IP model) coded in hardware description languages (HDL) is converted into one or more plurality of object libraries that are linked within an HDL simulator to execute system simulation." [0096]), but cannot be directly compiled to produce a practical hardware implementation of the electronic design (analogous to "IP protection is generally superior to any simulator specific model compiler, because simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty."[0072]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Jakubowski related to systems and methods for protecting digital goods, such as software with the teachings of Meyer related to a simulation method and apparatus, and, in particular, for converting and simulating electronic circuits coded in Hardware Description Languages (HDL). The motivation for doing so would have been more convenient to combine into one system simulation a plurality of subsystems HDL models created by different enterprises [0058].

Hence a skilled artisan having access to the teaching of Jakubowski and Meyer would have knowingly modified the teaching of Jakubowski with Meyer.

As per Claims 14 and 26:

The limitations of claims 14 and 26 have already been discussed in the rejection of Claim 2. They are therefore rejected under the same rationale.

As per Claims 15 and 27:

The limitations of claims 15 and 27 have already been discussed in the rejection of Claim 3. They are therefore rejected under the same rationale.

As per Claims 16 and 28:

The limitations of claims 16 and 28 have already been discussed in the rejection of Claim 4. They are therefore rejected under the same rationale.

As per Claims 17 and 29:

The limitations of claims 17 and 29 have already been discussed in the rejection of Claim 5. They are therefore rejected under the same rationale.

As per Claims 18 and 30:

The limitations of claims 18 and 30 have already been discussed in the rejection of Claim 6. They are therefore rejected under the same rationale.

As per Claims 19 and 31:

The limitations of claims 19 and 31 have already been discussed in the rejection of Claim 7. They are therefore rejected under the same rationale.

As per Claims 20 and 32:

The limitations of claims 20 and 32 have already been discussed in the rejection of Claim 8. They are therefore rejected under the same rationale.

As per Claims 21 and 33:

The limitations of claims 21 and 33 have already been discussed in the rejection of Claim 9. They are therefore rejected under the same rationale.

As per Claims 22 and 34:

The limitations of claims 22 and 34 have already been discussed in the rejection of Claim 10. They are therefore rejected under the same rationale.

As per Claims 23 and 35:

The limitations of claims 23 and 35 have already been discussed in the rejection of Claim 11. They are therefore rejected under the same rationale.

As per Claims 24 and 36:

The limitations of claims 24 and 36 have already been discussed in the rejection of Claim 12. They are therefore rejected under the same rationale.

As per Claim 25:

Jakubowski discloses a computer program product comprising a machine readable medium on which is provide program instructions comprising:

instruction for receiving a non-obfuscated version of the electronic design suitable for direct compilation to a practical hardware implementation of the electronic design (analogous to "The original digital good 122 represents the software product or data as originally produced, without any protection or code modifications." Col. 4 lines 5-7); and

instruction for adding obfuscation circuitry to produce an obfuscated version of the electronic design from which the simulation model can be created, wherein the obfuscation circuitry does not substantially impact the accuracy of the simulation results, but prevents practical implementation of the electronic design on a hardware device (analogous to "Generally speaking, the obfuscator 134 automatically parses the original digital good 122 and applies selected protection tools 136(1)-136(N) to various portions of the parsed good in a random manner to produce the protected digital good 124." Col. 3 lines 64-67; Fig. 1 element 134).

Jakubowski fails to disclose producing simulation model of an electronic design, which simulation model produces a hardware simulation result but cannot be directly compiled to produce a practical hardware implementation of the electronic design.

Meyer discloses producing a simulation model of an electronic design, which simulation model produces a hardware simulation result (analogous to "...electronic subsystem (soft IP model) coded in hardware description languages (HDL) is converted into one or more plurality of object libraries that are linked within an HDL simulator to execute system simulation." [0096]), but cannot be directly compiled to produce a practical hardware implementation of the electronic design (analogous to "IP protection is generally superior to any simulator specific model compiler, because simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty."[0072]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Jakubowski related to systems and methods for protecting digital goods, such as software with the teachings of Meyer related to a simulation method and apparatus, and, in particular, for converting and simulating electronic circuits coded in Hardware Description Languages (HDL). The motivation for doing so would have been more convenient to combine into one system simulation a plurality of subsystems HDL models created by different enterprises [0058]. Hence a skilled artisan having access to the teaching of Jakubowski and Meyer would have knowingly modified the teaching of Jakubowski with Meyer.

As per Claim 37:

Jakubowski discloses a method comprising:

(a) receiving a non-obfuscated version (analogous to "The original digital good 122 represents the software product or data as originally produced, without any protection or code modifications." Col. 4 lines 5-7);

(b) identifying a region of the non-obfuscated (analogous to "The process of selecting segments and augmenting them using various protection tools is repeated for many more segments...." Col. 7 lines 46-48);

(c) inserting entangler circuitry upstream from the region and inserting complementary detangler circuitry downstream from the region (analogous to "encryption/decryption" col. 12 lines 15-21);

(d) inserting scrambler circuitry upstream from the region and inserting complementary descrambler circuitry downstream from the region (analogous to

"Boolean Check Obfuscation" col. 12 lines 40 -67 and continue to col. 13 lines 1-26); and

Jakubowski fails expressly to disclose one or more flip-flops. However, this feature is, which is one or more flip-flops, deemed to be inherent to the Jakubowski system which stated as follows: "Separating detection and response makes it difficult for an attacker to discern what event or instruction set triggered the response." Col. 14 lines 36-38. Without having a flip-flop in the system of Jakubowski, it is impossible to triggered the response because a flip-flop is a trigger circuit.

Jakubowski fails expressly to disclose producing a simulation model, wherein the simulation model produces a hardware simulation result but cannot be directly compiled to produce a practical hardware implementation, and IP core in a native HDL format or in a partially compiled HDL format and optimizing the IP.

Meyer discloses producing a simulation model, wherein the simulation model produces a hardware simulation result (analogous to "...and electronic subsystem (soft IP model) coded in hardware description languages (HDL) is converted into one or more plurality of object libraries that are linked within an HDL simulator to execute system simulation." [0096]), but cannot be directly compiled to produce a practical hardware implementation (analogous to "IP protection is generally superior to any simulator specific model compiler, because simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty."[0072]), and IP core in a native HDL format or in a partially compiled HDL

format (analogous to "The final SoC system then comprises HDL descriptions from many sources. Such subcircuit or subsystem models are called Soft IP... " [0006] lines 4-8) and optimizing the IP core (analogous to "The preferred embodiment has the advantage that optimization and shrouding or obfuscation operation..." [0101] lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Jakubowski related to systems and methods for protecting digital goods, such as software with the teachings of Meyer related to a simulation method and apparatus, and, in particular, for converting and simulating electronic circuits coded in Hardware Description Languages (HDL). The motivation for doing so would have been more convenient to combine into one system simulation a plurality of subsystems HDL models created by different enterprises [0058]. Hence a skilled artisan having access to the teaching of Jakubowski and Meyer would have knowingly modified the teaching of Jakubowski with Meyer.

As per Claim 38:

Jakubowski discloses a method comprising:

(a) receiving a non-obfuscated version (analogous to "The original digital good 122 represents the software product or data as originally produced, without any protection or code modifications." Col. 4 lines 5-7);

(b) identifying a region of the non-obfuscated where one or more flip-flops are located (analogous to "The process of selecting segments and augmenting them using various protection tools is repeated for many more segments...." Col. 7 lines 46-48);

(c) inserting obfuscation circuitry into the region (analogous to "Generally speaking, the obfuscator 134 automatically parses the original digital good 122 and applies selected protection tools 136(1)-136(N) to various portions of the parsed good in a random manner to produce the protected digital good 124." Col. 3 lines 64-67);

Jakubowski fails expressly to disclose one or more flip-flops. However, this feature is, which is one or more flip-flops, deemed to be inherent to the Jakubowski system which stated as follows: "Separating detection and response makes it difficult for an attacker to discern what event or instruction set triggered the response." Col. 14 lines 36-38. Without having a flip-flop in the system of Jakubowski, it is impossible to triggered the response because a flip-flop is a trigger circuit.

Jakubowski fails expressly to disclose producing a simulation model, wherein the simulation model produces a hardware simulation result but cannot be directly compiled to produce a practical hardware implementation of the IP core, and IP core in a native HDL format or in a partially compiled HDL format and optimizing the IP.

Meyer discloses producing a simulation model, wherein the simulation model produces a hardware simulation result (analogous to "...and electronic subsystem (soft IP model) coded in hardware description languages (HDL) is converted into one or more plurality of object libraries that are linked within an HDL simulator to execute system simulation." [0096]), but cannot be directly compiled to produce a practical hardware implementation of the IP core (analogous to "IP protection is generally superior to any simulator specific model compiler, because simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to

shroud and/or obfuscate the object code without increasing simulator development difficulty."[0072]), and IP core in a native HDL format or in a partially compiled HDL format (analogous to "The final SoC system then comprises HDL descriptions from many sources. Such subcircuit or subsystem models are called Soft IP... " [0006] lines 4-8) and optimizing the IP core (analogous to "The preferred embodiment has the advantage that optimization and shrouding or obfuscation operation..." [0101]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Jakubowski related to systems and methods for protecting digital goods, such as software with the teachings of Meyer related to a simulation method and apparatus, and, in particular, for converting and simulating electronic circuits coded in Hardware Description Languages (HDL). The motivation for doing so would have been more convenient to combine into one system simulation a plurality of subsystems HDL models created by different enterprises [0058]. Hence a skilled artisan having access to the teaching of Jakubowski and Meyer would have knowingly modified the teaching of Jakubowski with Meyer.

Conclusion

17. Claims 1-39 are rejected.

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 7,080,257 issued to Jakubowski et al discloses an obfuscator which configure to transform an original digital good into protected digital code.

US Patent No. 7,065,652 issued to Xu et al discloses a method for obfuscating computer program instructions upon disassembly, the method comprising inserting an obfuscating instruction or causing a disassembler to not disassemble one or more bytes subsequent to the obfuscating instruction.

M. Gomathisankaran, and A. Tyagi, "Architecture Support for 3D Obfuscation", discloses to develop an architecture to support 3-D obfuscation through the use of well known cryptographic methods.

C. S. Collberg, C. Thomborson, "Watermarking, Tamper-Proofing, and Obfuscation-Tools for Software Protection" IEEE Transaction on Software Engineering, Vol. 28, No. 8, August 2002, discloses a defense against reverse engineering which is obfuscation.

19. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kamini shah can be reached at (571) 272-2279. The official fax number is

(571) 273-8300. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

Kibrom K. Gebresilassie
Patent Examiner
U.S. Patent and Trademark Office
Simulation and Emulation, Art Unit 2128
401 Dulany St., Room 5C25 (Randolph)
Alexandria, VA 22314-5774
Tel: 571-272-8571
Kibrom.gebresilassie@uspto.gov

KAMINI SHAH
SUPERVISORY PATENT EXAMINER